CLAIMS

1-23. (Cancelled)

24. (Currently Amended) A multistage differential amplifier comprising:

a first amplifier stage, the first amplifier stage including:

a first differential pair of input NPN bipolar transistors with loads coupled to a supply voltage through a first common-mode PMOS transistor; and

~~(ii)~~ a first pair of emitter-follower output NPN bipolar transistors coupled to the first differential pair of input transistors;

a second amplifier stage, the second amplifier stage including:

a second differential pair of input transistors with loads coupled to the supply voltage through a second common-mode transistors; and

a second pair of emitter-follower output transistors coupled to the second differential pair of input transistors, wherein the second differential pair of input transistors is coupled to the first pair of emitter-follower output transistors; and

a voltage regulator coupled to control ~~said~~ the first common-mode transistor, the voltage regulator including:

a differential amplifier with a first input from a reference voltage, a second input from a temperature responsive unit, and an output to a third transistor connected between a supply voltage and the temperature responsive unit; and

a regulated voltage output node between the third transistor and the temperature responsive unit, wherein the temperature responsive unit includes in series a first resistor, a second resistor, and a diode-connected NPN bipolar transistor.

25. (Previously Presented) The amplifier of claim 24, wherein the voltage regulator is coupled to control the second common-mode transistor.

26. (Previously Presented) The amplifier of claim 25, further comprising a third amplifier stage, the third amplifier stage including:

a third differential pair of input transistors with loads coupled to the supply voltage

through a third common-mode transistor; and

a third pair of emitter-follower output transistors coupled to the third differential pair of input transistors, wherein ~~said~~ the third differential pair of input transistors is coupled to the second pair of emitter-follower output transistors.

27-28. (Cancelled)